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IN THE CLAIMS:

Kindly cancel claims 17-42, 47-53, 55-73, 83, 84, 88 and 91 without prejudice or admission, and amend claims 1, 3-10, 12-14, 43, 85, 89 and 92 as shown in the following listing of claims, which replaces all previous versions and listings of claims.

1. (currently amended) A complementary MOS semiconductor device, comprising: a semiconductor substrate; a CMOS transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and a P-channel enhancement mode MOS transistor having a threshold voltage of approximately -0.5V and a surface channel formed in the semiconductor substrate, the N-channel MOS transistor and the P-channel MOS transistor forming a complementary transistor pair; and a resistor formed on ~~in~~ the semiconductor substrate; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

2. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a single layer of polycrystalline silicon having a film

thickness in a range of 2000 Å to 6000 Å and including boron or BF_2 with an impurity concentration of at least 1 x 10^{19} atoms/cm^3.

3. (currently amended) A complementary MOS semiconductor device according to claim 1~~;~~ ~~,~~ wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each have a polycide structure comprising a lamination of a ~~first~~ polycrystalline silicon layer having a film thickness in a range of 1000 Å to 4000 Å and including boron or BF_2 with an impurity concentration of 1 x 10^{19} atoms/cm^3 or more and a ~~first~~ high melting point metal silicide layer selected from the group consisting of molybdenum silicide, tungsten silicide, titanium silicide, and platinum silicide, with a film thickness in a range of 500 Å to 2500 Å.

4. (currently amended) A complementary MOS semiconductor device according to ~~of~~ claim 1; wherein the resistor is a polycrystalline silicon resistor formed in the same layer and having the same film thickness range as ~~the~~ polycrystalline silicon constituting the gate electrodes of the N-type transistor and the P-type transistor.

5. (currently amended) A complementary MOS semiconductor device according to claim 1~~;~~ ~~,~~ wherein the

resistor is formed of a ~~second~~ polycrystalline silicon layer having a film thickness in a range of 500 Å to 2000 Å.

6. (currently amended) A complementary MOS semiconductor device according to claim 1, wherein the resistor is a thin metal transistor formed from a material ~~one~~ selected from the group consisting of Ni-Cr alloy, Cr-SiO alloy, molybdenum silicide, and ß-ferrite silicide ~~silicde~~ and has a film thickness in a range of 100 Å to 300 Å.

7. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~,~~ wherein the resistor comprises a ~~comprising the first or the second~~ polycrystalline silicon layer containing ~~contains~~ phosphorous or arsenic with an impurity concentration of $1x10^{14}$ to $9x10^{18}$ atoms/cm^3 and includes an ~~a first~~ N-type transistor of a relatively low concentration having a sheet resistance in the range ~~in an order~~ of several kΩ/square to several tens of KΩ/square.

8. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~,~~ wherein the resistor comprises a ~~comprising the first or the second~~ polycrystalline silicon layer containing ~~contains~~ phosphorous or arsenic with an impurity concentration of $1x10^{19}$ atoms/cm^3 or more and includes an ~~a second~~ N-type transistor of a

relatively high concentration having a sheet resistance in the range ~~in an order~~ of about 100 Ω/square to several hundreds of Ω/square and a temperature coefficient in the range ~~an order~~ of several hundreds of ppm/°C to about 1000 ppm/°C.

9. (currently amended) A complementary MOS semiconductor device according to claim 1~~;~~ ~~,~~ wherein the resistor comprises a ~~comprising the first or the second~~ polycrystalline silicon layer containing ~~contains~~ boron or BF_2 with an impurity concentration of $1x10^{14}$ to $9x10^{18}$ atoms/cm^3 and includes a ~~first~~ P-type transistor of a relatively low concentration having a sheet resistance in the range ~~in an order~~ of several kΩ/square to several tens of kΩ/square.

10. (currently amended) A complementary MOS semiconductor device according to claim 1~~;~~ ~~,~~ wherein the resistor comprises a ~~comprising the first or the second~~ polycrystalline silicon layer containing ~~contains~~ boron or BF_2 with an impurity concentration of $1x10^{19}$ atoms/cm^3 or more and includes a ~~second~~ P-type transistor of a relatively high concentration having a sheet resistance in the range ~~in an order~~ of several hundreds of Ω/square to about 1 kΩ/square and a temperature coefficient in the range ~~in an order~~ of several hundreds of ppm/°C to about 1000 ppm/°C.

11. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the N-channel MOS transistor and the P-channel MOS transistor have a single drain structure comprising a diffusion layer with a high impurity concentration, and a source and a drain of the N-channel MOS transistor and the P-channel MOS transistor overlap the P-type gate electrode in a planar manner.

12. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~,~~ wherein the N-channel MOS transistor and the P-channel MOS transistor ~~include a MOS transistor having a second structure comprising~~ each have a diffusion layer with a low impurity concentration and with at least one of a source side and a drain side thereof that overlaps ~~in which only the drain side thereof overlaps the P-type gate electrode in a planar manner or both the source and drain sides thereof overlap~~ the P-type gate electrode in a ~~the~~ planar manner, and a diffusion layer with a high impurity concentration and having at least one of a source side and a ~~in which only the~~ drain side thereof that does not overlap the P-type gate electrode in a ~~the~~ planar manner ~~or both the source and drain sides thereof do not overlap the P-type gate electrode in the planar manner~~.

13. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~,~~ wherein the N-channel MOS transistor and the P-channel MOS transistor each include a ~~MOS transistor having a third structure comprising a~~ diffusion layer with a low impurity concentration and having at least one of a source side and a drain side thereof that overlaps ~~in which only the drain side thereof overlaps the P-type gate electrode in a planar manner or both the source and drain side thereof overlap~~ the P-type gate electrode in a ~~the~~ planar manner and a diffusion layer with a high impurity concentration and having at least one of a source side and a drain side thereof that does ~~in which only the drain side thereof does not overlap the P-type gate electrode in the planar manner or both the source and drain sides thereof do~~ not overlap the P-type gate electrode in a ~~the~~ planar manner, and an insulating film between the diffusion layer with a high impurity concentration and the P-type gate electrode and having ~~has~~ a larger film thickness ~~thicker~~ than that of a gate insulating film.

14. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~,~~ wherein the N-channel MOS transistor and the P-channel MOS transistor ~~include a MOS transistor having a fourth structure comprising~~ each have a diffusion layer with a high impurity concentration

and having ~~in which both the~~ source and the drain sides that overlap the P-type gate electrode in a planar manner, and a diffusion layer with a low impurity concentration with at least a ~~in which only the~~ drain side thereof ~~or both the source and drain sides thereof~~ that is diffused ~~diffuse~~ further on a ~~the~~ channel side to overlap the P-type gate electrode in a ~~the~~ planar manner.

15. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the N-channel MOS transistor has a buried channel and a threshold voltage in an enhancement mode.

16. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the P-channel MOS transistor has a surface channel and a threshold voltage in an enhancement mode.

17. - 42. (canceled).

43. (currently amended) A complementary MOS semiconductor device according to claim 1; wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming ~~formed in~~ an N-type well ~~in the semiconductor substrate~~.

44. (previously presented) A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

45. (previously presented) A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming a P-type well, respectively.

46. (previously presented) A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS trnansistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

47. - 53. (canceled).

54. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the polycrystalline silicon is formed by chemical vapor deposition.

55. - 73. (canceled).

74. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a single layer of polycrystalline silicon.

75. (previously presented) A complementary MOS semiconductor device according to claim 74; wherein film thickness of the polycrystalline silicon layer is in the range of 2000 angstroms to 6000 angstroms.

76. (previously presented) A complementary MOS semiconductor device according to claim 74; wherein the polycrystalline silicon layer has a concentration of boron or BF_2 in a concentration of at least 1×10^{19} atoms/cm^3.

77. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a polycide structure comprising a polycrystalline silicon layer and a high melting point metal silicide layer formed thereover.

78. (previously presented) A complementary MOS semiconductor device according to claim 77; wherein the high melting point metal silicide layer is formed of at least one metal silicide selected from the group consisting of molybdenum silicide, tungsten silicide, titanium silicide and platinum silicide.

79. (previously presented) A complementary MOS semiconductor device according to claim 77; wherein the high melting point metal silicide layer has a thickness in the range of 500 angstroms to 2500 angstroms.

80. (previously presented) A complementary MOS semiconductor device according to claim 77; wherein the resistor is a polycrystalline silicon resistor formed from the same polycrystalline silicon layer and having the same thickness as that of the polycrystalline silicon layer of the gate electrodes of the N-channel MOS transistor and the P-channel MOS transistor.

81. (previously presented) A complementary MOS semiconductor device according to claim 77; wherein the resistor is a polycrystalline silicon resistor formed of a polycrystalline silicon film having a thickness in the range of 500 angstroms to 2000 angstroms.

82. (previously presented) A complementary MOS semiconductor device according to claim 77; wherein the resistor is a thin film transistor.

83. (canceled).

84. (canceled).

85. (currently amended) A complementary MOS semiconductor device according to claim 1; ~~84;~~ wherein the N-channel MOS transistor is an enhancement mode transistor having a buried channel.

86. (previously presented) A complementary MOS semiconductor device according to claim 85; wherein a threshold voltage of the N-channel MOS transistor is set using arsenic as a donor impurity so that the buried channel is a shallow buried channel.

87. (previously presented) A complementary MOS semiconductor device according to claim 1; wherein the N-channel MOS transistor is used in a reference voltage generating circuit of a voltage regulator and the P-channel MOS transistor is used as an output driving transistor of the voltage regulator.

88. (canceled).

89. (currently amended) A complementary MOS semiconductor device for a voltage regulator having a reference voltage generating circuit, an error amplifier, an output driving transistor and a voltage divider, the complementary MOS semiconductor device comprising: a semiconductor substrate; a complementary transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and a P-channel MOS transistor <u>having a threshold voltage of approximately -0.5V</u> formed in the semiconductor substrate, one of the complementary transistors serving as the output driving transistor of the voltage regulator; and a resistor formed in the semiconductor substrate and used in the voltage divider; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

90. (previously presented) A complementary MOS semiconductor device according to claim 89; wherein the P-channel MOS transistor is an enhancement mode transistor having a surface channel.

91. (canceled).

92. (currently amended) A complementary MOS semiconductor device according to claim 89; ~~91;~~ wherein the N-channel MOS transistor is an enhancement mode transistor having a buried channel.

93. (previously presented) A complementary MOS semiconductor device according to claim 92; wherein a threshold voltage of the N-channel MOS transistor is set using arsenic as a donor impurity so that the buried channel is a shallow buried channel.